***In the Claims***

Claims remaining in the application are as follows:

1. (Original): A circuit for connection to a backplane connector interfacing with a bus, where the bus may carry a diffsense signal, and where the circuit may connect to a voltage source comprising:

a comparator, comprising a comparator output configured as an open collector;

a pullup resistor having two terminals, where one said terminal is connected to said comparator output and the other said terminal is connected to the voltage source; and

a programmable logic device having an interface, said interface electrically connected to said terminal of said pullup resistor connected to said comparator output, whereby a diffsense prime signal is generated by the combination of said comparator output and said programmable logic device interface.

2. (Original): The circuit of claim 1, wherein said comparator comprises:

a noninverting input connected to the backplane connector, wherein the diffsense signal is applied to said noninverting input;

an inverting input, wherein a substantially fixed voltage is applied to said inverting input; and a switchable connection to ground.

3. (Original): The circuit of claim 1, wherein said programmable logic device comprises:

a tri-state buffer having an input, an output and a control terminal, wherein said output of said buffer is connected to said interface and said input is connected to ground; and

transceiver disable logic connected to said control terminal of said tri-state buffer.

4. (Original): The circuit of claim 3, further comprising at least one conductor electrically connected to said transceiver disable logic, whereby at least one signal can be transmitted to said transceiver disable logic.

5. (Original): The circuit of claim 3, further comprising:

an input element connected to said output of said tri-state buffer; and

expander enable logic electrically connected to said input element.

6. (Original): The circuit of claim 5, further comprising an expander, wherein said expander enable logic is electrically connected to said expander.

7. (Original): The circuit of claim 1, wherein said voltage source is at logic high voltage.

8. (Original): The circuit of claim 7, wherein said voltage source is substantially at five volts.

9. (Original): The circuit of claim 1, further comprising a voltage divider connected to said inverting input of said comparator, wherein said voltage divider applies said substantially fixed voltage to said inverting input.

10. (Original): The circuit of claim 1, wherein said substantially fixed voltage applied to said inverting input of said comparator is substantially 2.4 volts.

11. (Original): The circuit of claim 1, further comprising a transceiver electrically connected to said interface of said programmable logic device and to said terminal of said pullup resistor connected to said comparator output.

12. (Original): A bus controller card for use with a backplane having a bus controller slot connected to a bus, comprising:

a backplane connector, wherein said backplane connector is detachably connected to said bus controller slot;

a controller electrically connected to said backplane connector, said controller comprising

a comparator, comprising

a noninverting input connected to the backplane connector, wherein the diffsense signal is applied to said noninverting input,

an inverting input, wherein a substantially fixed voltage is applied to said inverting input, and

a comparator output configured as an open collector;

a pullup resistor having two terminals, where one said terminal is connected to said comparator output and the other said terminal is connected to the voltage source; and

a programmable logic device comprising

an interface electrically connected to said terminal of said pullup resistor connected to said comparator output,

a tri-state buffer having an input, an output and a control terminal, wherein said output of said buffer is connected to said interface and said input is connected to ground,

transceiver disable logic connected to said control terminal of said tri-state buffer,

an input element connected to said output of said tri-state buffer, and

expander enable logic electrically connected to said input element;

an expander electrically connected to said expander enable logic; and

a high voltage differential transceiver electrically connected to said interface of said programmable logic device and to said terminal of said pullup resistor connected to said comparator output, whereby a diffsense prime signal is generated by the combination of said comparator output and said programmable logic device interface.

13. (Currently amended): A method for controlling a device connected to a bus, comprising:

checking for a diffsense signal from the bus;

comparing the diffsense signal to a reference voltage;

generating a diffsense prime signal based on said comparing; ~~and~~

selectively modifying said generated diffsense prime signal;

transmitting said selectively modified diffsense prime signal to the device; and

switching the device off in response to asserting said diffsense prime signal low.

Claims 14-15 (canceled).

16. (Currently amended): A method for controlling a device comprising:
determining whether a diffsense signal on a bus is within a specified diffsense voltage range associated with a differential bus;
generating a diffsense prime signal based on the determination;
selectively modifying the diffsense prime signal; and
selectively activating and deactivating a the device based on the ~~determination~~ modified diffsense prime signal.

17. (Previously presented): The method according to claim 16 further comprising:
determining whether a diffsense signal on a bus is within a voltage range associated with a high-voltage differential (HVD) small computer systems interface (SCSI) bus.

18. (Previously presented): The method according to claim 16 wherein:
the device is a high-voltage differential (HVD) transceiver.